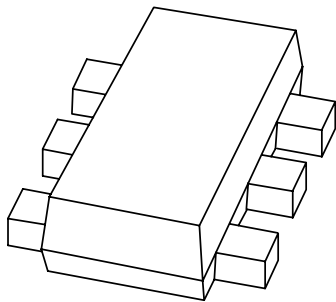


DATA SHEET



PBSS2515VS

15 V low V_{CEsat} NPN double
transistor

Product specification
Supersedes data of 2001 Sep 13

2001 Nov 07

15 V low V_{CEsat} NPN double transistor

PBSS2515VS

FEATURES

- 300 mW total power dissipation
- Very small 1.6 x 1.2 mm ultra thin package
- Excellent coplanarity due to straight leads
- Low collector-emitter saturation voltage
- High current capability
- Improved thermal behaviour due to flat lead
- Replaces two SC-75/SC-89 packaged low V_{CEsat} transistors on same PCB area
- Reduces required PCB area
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and muting
- Low frequency driver circuits
- LCD backlighting
- Audio frequency general purpose amplifier applications
- Battery driven equipment (mobile phones, video cameras and hand-held devices).

DESCRIPTION

NPN low V_{CEsat} double transistor in a SOT666 plastic package.
 PNP complement: PBSS3515VS.

MARKING

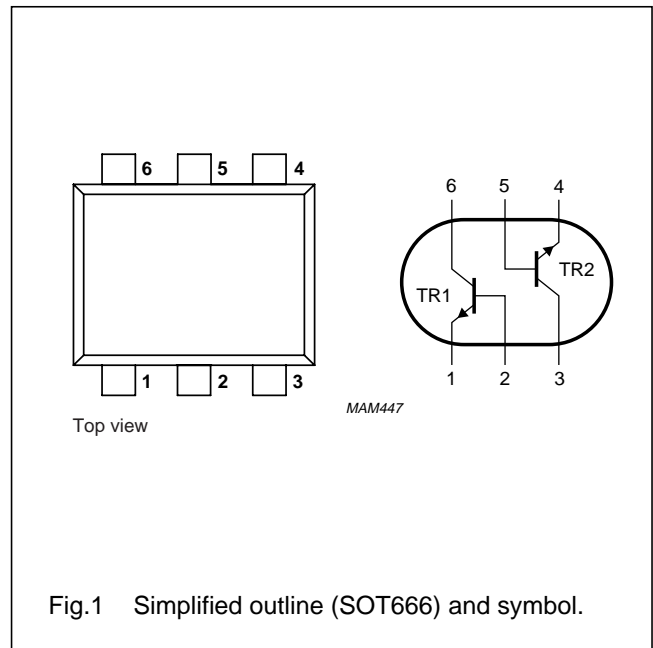
TYPE NUMBER	MARKING CODE
PBSS2515VS	N9

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	15	V
I_{CM}	peak collector current	1	A
R_{CEsat}	equivalent on-resistance	<500	m Ω

PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



15 V low V_{CEsat} NPN double transistor

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor unless otherwise specified					
V_{CBO}	collector-base voltage	open emitter	–	15	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
V_{EBO}	emitter-base voltage	open collector	–	6	V
I_C	collector current (DC)		–	500	mA
I_{CM}	peak collector current		–	1	A
I_{BM}	peak base current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		65	+150	°C
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	300	mW

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	notes 1 and 2	416	K/W

Notes

1. Transistor mounted on an FR4 printed-circuit board.
2. The only recommended soldering method is reflow soldering.

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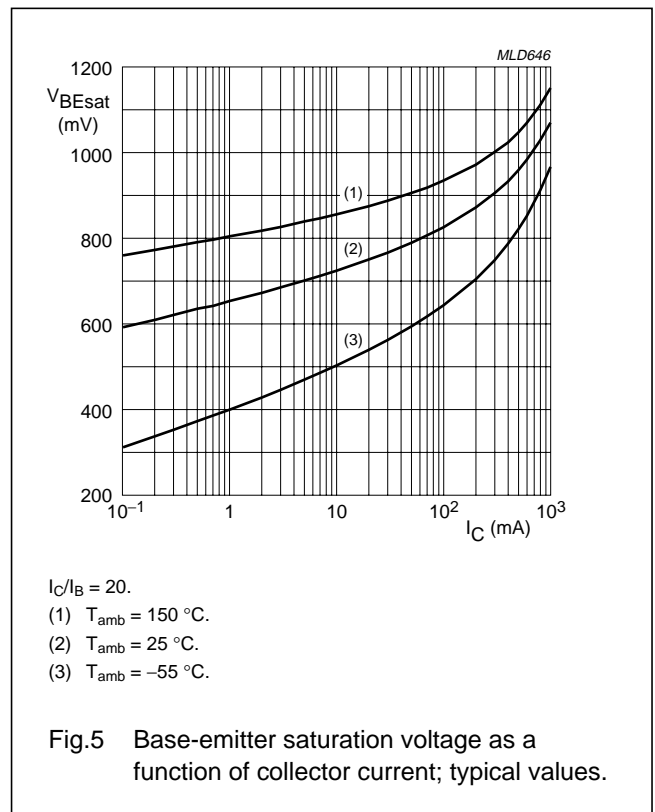
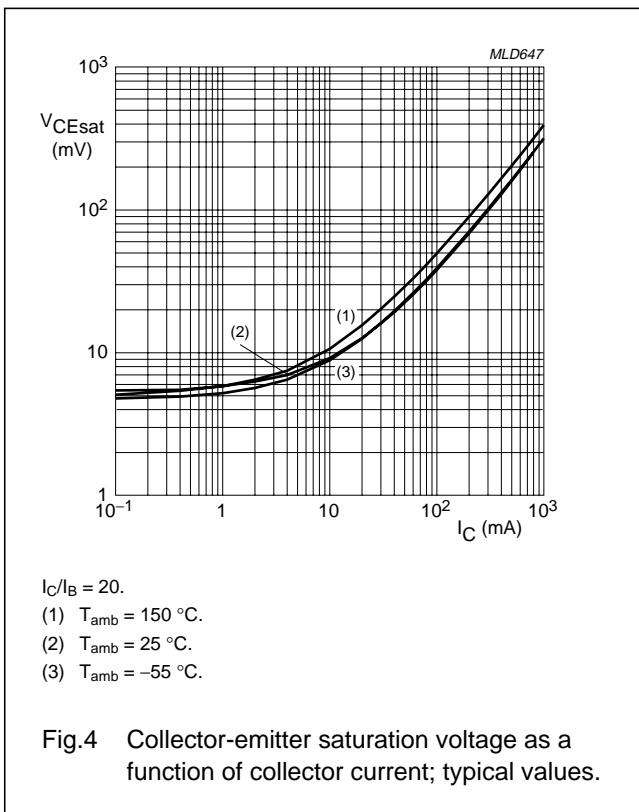
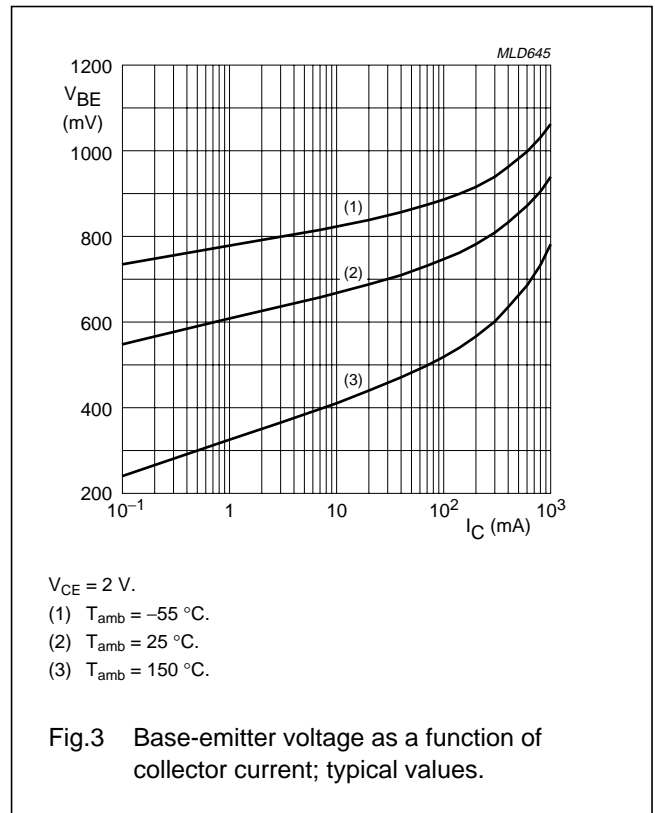
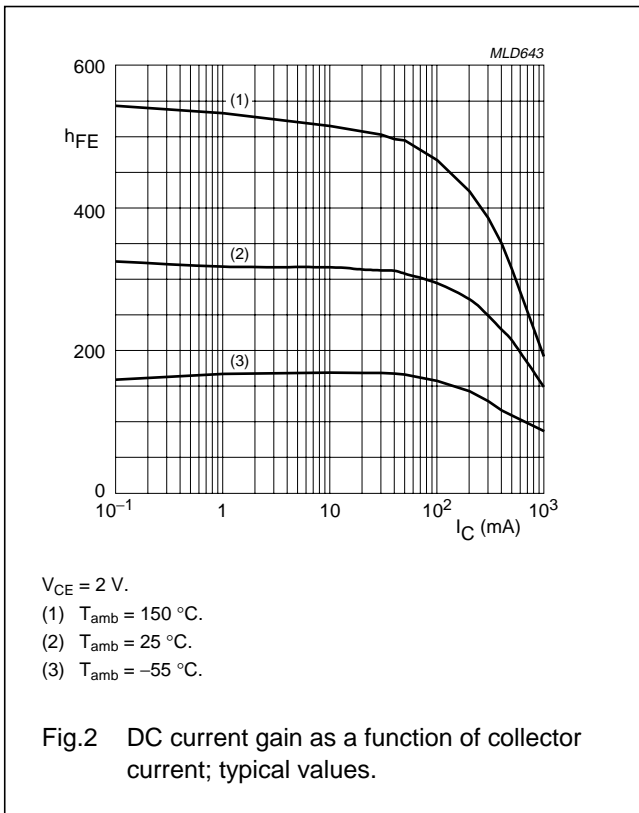
CHARACTERISTICS $T_{amb} = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor unless otherwise specified						
I_{CBO}	collector-base cut-off current	$V_{CB} = 15\text{ V}; I_E = 0$	–	–	100	nA
		$V_{CB} = 15\text{ V}; I_E = 0; T_j = 150\text{ °C}$	–	–	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0$	–	–	100	nA
h_{FE}	DC current gain	$V_{CE} = 2\text{ V}; I_C = 10\text{ mA}$	200	–	–	
		$V_{CE} = 2\text{ V}; I_C = 100\text{ mA};$ note 1	150	–	–	
		$V_{CE} = 2\text{ V}; I_C = 500\text{ mA};$ note 1	90	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	–	–	25	mV
		$I_C = 200\text{ mA}; I_B = 10\text{ mA}$	–	–	150	mV
		$I_C = 500\text{ mA}; I_B = 50\text{ mA};$ note 1	–	–	250	mV
R_{CEsat}	equivalent on-resistance	$I_C = 500\text{ mA}; I_B = 50\text{ mA};$ note 1	–	300	<500	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = 500\text{ mA}; I_B = 50\text{ mA};$ note 1	–	–	1.1	V
V_{BE}	base-emitter turn-on voltage	$V_{CE} = 2\text{ V}; I_C = 100\text{ mA};$ note 1	–	–	0.9	V
f_T	transition frequency	$I_C = 100\text{ mA}; V_{CE} = 5\text{ V}; f = 100\text{ MHz}$	250	420	–	MHz
C_C	collector capacitance	$V_{CB} = 10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$	–	4.4	6	pF

Note1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$.

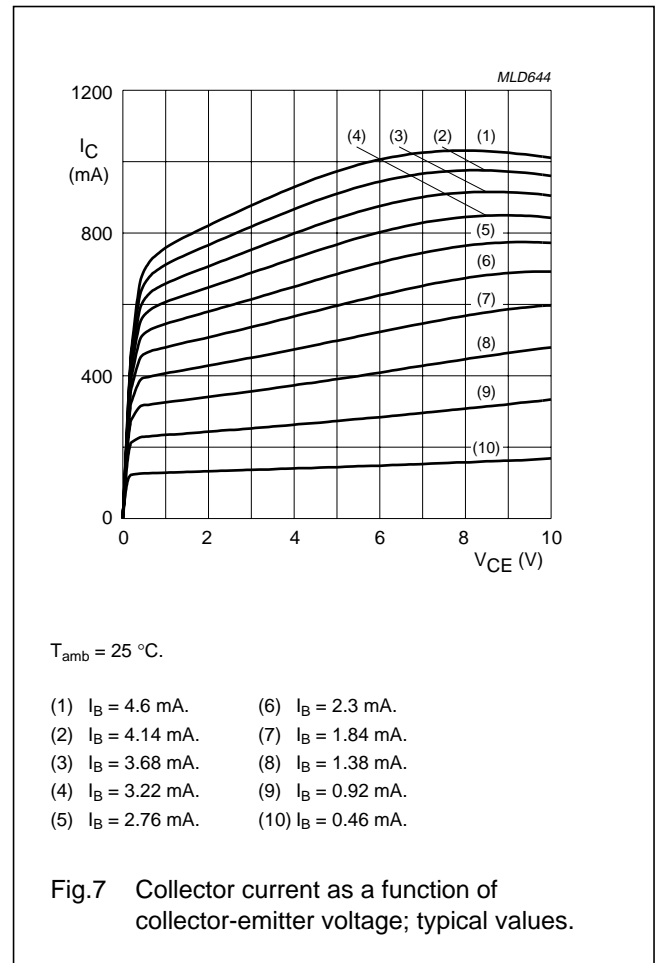
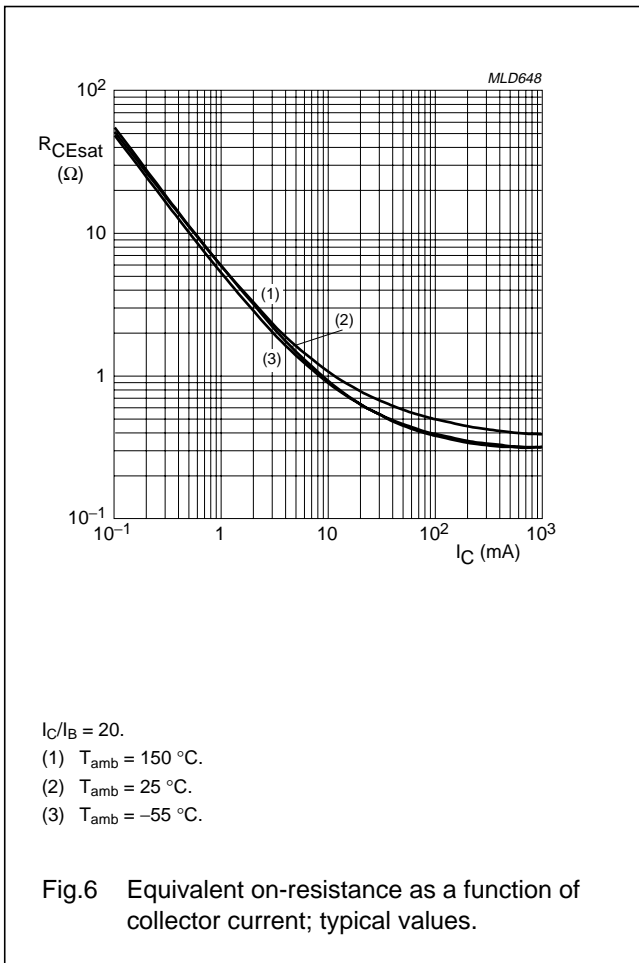
15 V low V_{CEsat} NPN double transistor

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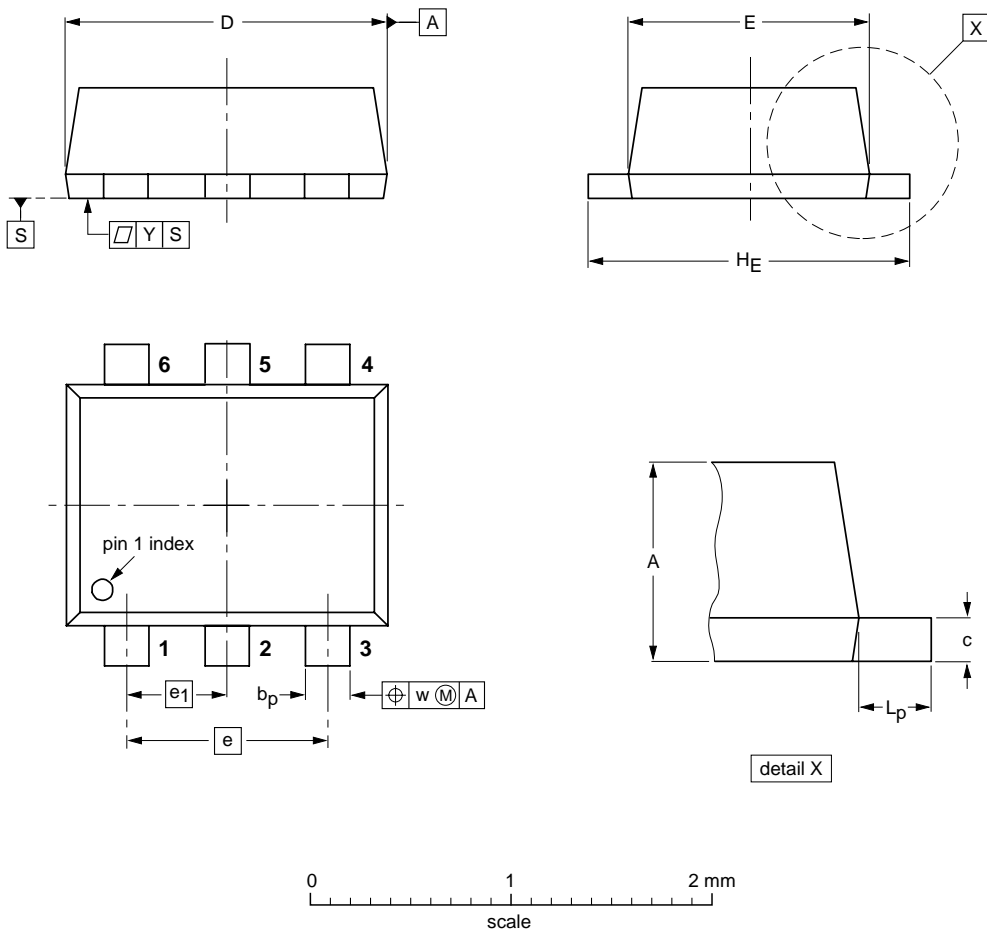
15 V low V_{CEsat} NPN double transistor

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						01-01-04 01-08-27

15 V low V_{CEsat} NPN double transistor

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DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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NOTES

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NOTES

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